A MOSFET Design Laboratory Course

Ahmet Bindal, *Member IEEE*, Salih Kilic and Lili He
ahmet.bindal@sjsu.edu

***Abstract*—**The authors have developed a graduate level MOSFET design laboratory course at San Jose State University using Silvaco's device design tools and simulation platform. The laboratory experiments explain the design methodology of an enhancement type NMOS and a depletion type PMOS transistor. The technology specifying the power supply voltage to be applied to the gate and the drain of the transistor, the gate oxide thickness, on and off drain currents and the threshold voltage (Vt) at the minimum effective channel length are provided to students as the starting point of the design. Using Silvaco's Atlas Design Environment, students begin exploring various channel-doping profiles to obtain the specified Vt for both NMOS and PMOS transistors at the minimum effective channel length. Next, the Vt-drop off as the result of the charge sharing in the channel is investigated as the effective channel length is increased towards 1 micron from the minimum geometry. Students analyze the effect of the high electric field at the drain in terms of avalanche breakdown by measuring the substrate current and employ Lightly Doped Drain (LDD) for both NMOS and PMOS transistors in order to reduce it. At this point, students change the LDD doping, depth and length and record the resultant substrate current versus transconductance (gm) of the device at the minimum effective channel length to select the best NMOS and PMOS transistors. The subsequent tasks determine the device's subthreshold slope to specify how fast the transistor turns on and its body-effect characteristics for increasing substrate voltages. The device design experiments are concluded with plotting the gate-source, gate-drain, gate-substrate, drain-substrate and source-substrate capacitance values as a function of applied voltage. In remaining part of the semester, students use Silvaco's Athena Design Environment to do process simulation on the designed NMOS and PMOS devices. After specifying the complete process flow and the annealing temperatures used, the n-type and p-type doping profiles in the channel, the LDD region and the source/drain contacts are replicated by experimenting various Arsenic (Phosphorous) and Boron implantation dose and energy values. Subsequently, students use these new doping profiles and device structures obtained as the result of process simulation and re-determine the NMOS and PMOS threshold voltages at different effective channel lengths, substrate currents to monitor the effect of LDD against avalanche breakdown, subthreshold slope, body-effect and device capacitances. Differences in device characteristics before and after process simulation are recorded to illustrate the effect of a non-ideal scenario.